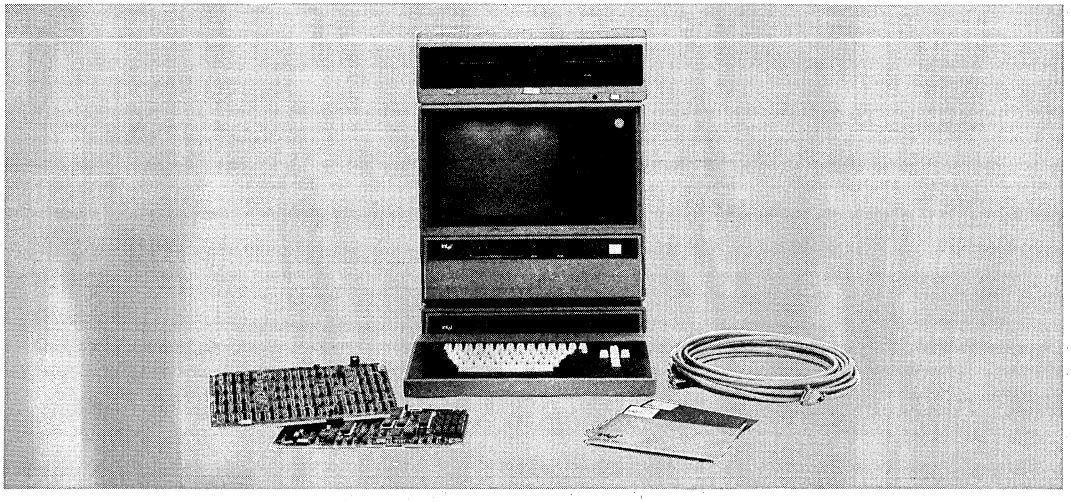
MODEL 675
INTELLEC® DEVELOPMENT SYSTEM
FOR ETHERNET* DS/E

- **Complies with the Intel, DEC, and Xerox Tricompany Ethernet Specification**
- **Provides a complete Ethernet Communications Development System Environment**
- **Includes an Ethernet Data Link Layer Software Library to allow user programs to access the Ethernet Data Link from the 8085 in Model 675 systems**
- **Supports the Ethernet Data Link and Physical Link Control via the MULTIBUS Ethernet Communications Controller**
- **Includes a special 10 meter Interconnect Cable for connecting two Model 675s for Ethernet software prototyping**
- **Supports the full range of iAPX 86, 88-resident, High-Level Languages: PL/M 86/88; PASCAL 86/88; and FORTRAN 86/88**
- **Includes a Software Applications Debugger for iAPX 86, 88 user programs**
- **Upgradable from Intellec Series II/85 and Series III**

The Intellec Development System for Ethernet (DS/E) provides the user with the tools necessary to develop and test communication software and applications that will use Ethernet as a communication subsystem. It combines the power of the Intellec Microcomputer Development System with a dual board Ethernet Communications Controller for microprocessor development. This combination allows the user to develop either 8- or 16-bit Ethernet-based applications.

The Ethernet Communications Controller incorporates the Ethernet Data Link and Physical Link Control to meet the Ethernet specification for 10 Mbit per second data transmission rate over coaxial cable. The controller consists of two MULTIBUS compatible boards, the Processor board and the Serialization/Deserialization (SerDes) board. The Processor board provides the function of packet buffering, processing, and transferring of the processed packets to system memory. The SerDes board performs the serialization/deserialization, framing, CRC generation and checking, Manchester encoding/decoding, and destination address recognition. A 10 meter interconnect cable is included to permit two Model 675s to be connected in a functioning Ethernet environment without the need for Ethernet transceivers and coaxial cable.

*Ethernet is a trademark of Xerox Corporation.



COMPONENTS

Hardware Components

The Model 675 consists of a CRT chassis with a 6-slot cardcage, power supply, fans, cables, single floppy diskette drive, a detachable upper/lower case full ASCII keyboard, and six printed circuit boards. A block diagram of the Model 675 is shown in Figure 1.

System Components

Two CPU boards, the IPC-85 and the RPB-86, reside on the Model 675 MULTIBUS system bus, each containing its own microprocessor, memory, I/O, interrupt and bus interface circuitry implemented with Intel's high technology LSI components. The IPC-85 integrated processor board consists of an Intel NMOS 8-bit microprocessor, the 8085A-2, and 64 Kbytes of on board memory. The RPB-86 resident processor board contains Intel's HMOS 16-bit microprocessor, the iAPX 86 (8086), and 64 Kbytes of on board memory.

A third CPU board, known as the I/O controller (IOC) performs all remaining I/O including the interface to the CRT, integral floppy disk, and keyboard. The IOC contains its own microprocessor, RAM and ROM memory, and I/O interface logic. It is a slave CPU board which communicates with the IPC-85 over an 8-bit bidirectional data bus.

The Model 675 also includes an additional 64 Kbyte MULTIBUS compatible RAM board supplying the user with a total of 192 Kbytes of RAM. The two remaining boards are the Ethernet Communications Controller.

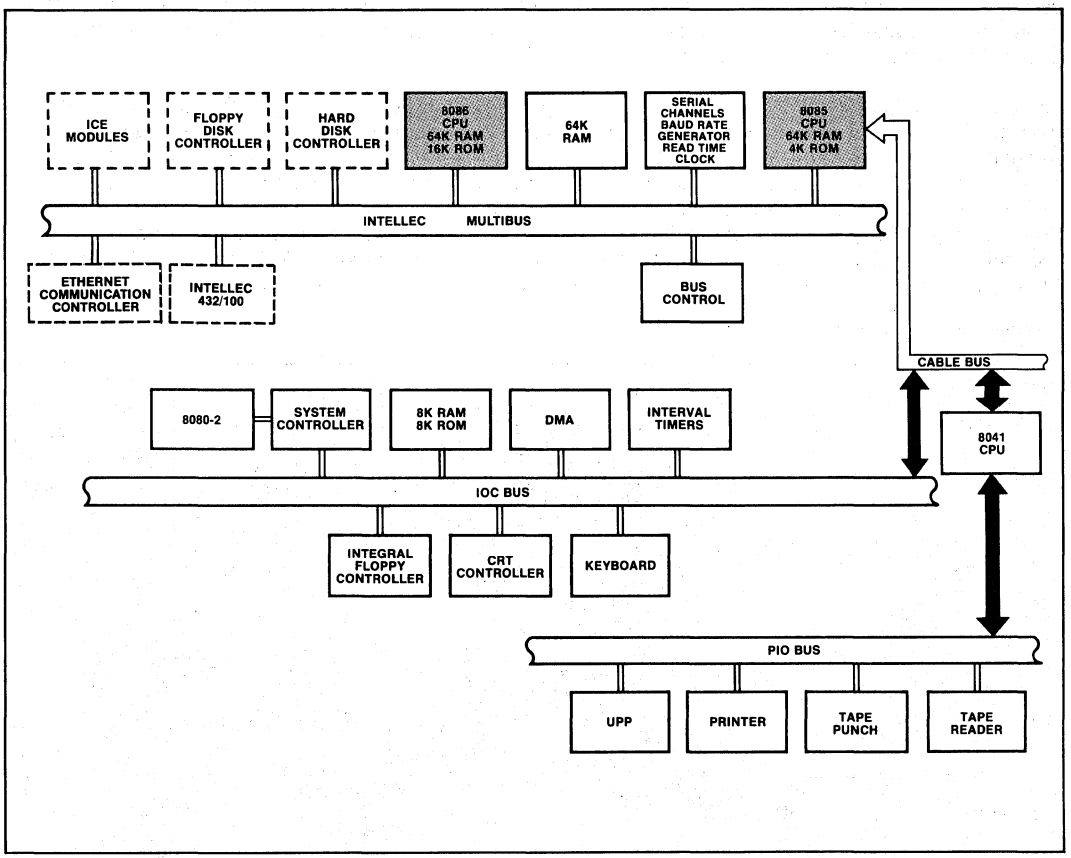


Figure 1. Model 675 DS/E Block Diagram

Expansion

The Intellec expansion chassis Model 201 is included in the basic Model 675. All Model 675 systems contain 10 MULTIBUS board slots—6 in the main system and 4 in the Model 201 chassis. The table below indicates the number of slots available for expansion in each.

Model	Available Expansion Slots
675	4
675FD	2
675HD	2

Ethernet Communications Controller

PROCESSOR BOARD

The processor board interfaces to the MULTIBUS system bus and contains the Intel 5 MHz 8088 CPU, 16 Kbytes dynamic RAM for Ethernet and host interface program execution, 8K EPROM pre-programmed for the Data Link Control, and an 8K static RAM for transmit and receive channel DMA data buffering. The Processor board provides the necessary commands and control to the SerDes board and receives status and data from it.

SerDes BOARD

The SerDes board meets the required electrical specification to the transceiver and provides the Data Link Layer of the Ethernet architecture. The major functions of the SerDes board include serialization/deserialization, framing, Manchester encoding/decoding, transmit data flow control, receive data flow control, destination address decoding for received message, CRC generation and checking, and diagnostic for CRC error, loopback, transmit timeout, and if used with transceivers, CSMA/CD (carrier-sense multiple-access with collision-detection).

DATA BUFFERING

All data transfers from the Ethernet Data Link control of the SerDes board are buffered through the 8K static RAM. This minimizes the amount of bus time used by the Ethernet Communications Controller by eliminating the possibility of data overruns and subsequent repeated I/O operations. In addition, the buffer allows the Ethernet Communications Controller to have a bus priority below higher-priority, time-critical parts of the system.

DIAGNOSTICS

Diagnostic functions are resident on the SerDes board and can be invoked on demand by the program on the Processor board. These functions incude: transmitting packets with a bad CRC; receiving all packets regardless of address; reading data received in error; SerDes loop-back, this function allows data from static RAM to be transmitted and received simultaneously (the received data is verified but not written to the Static RAM). The CRC generation and checking can be used to verify transmit and receive data.

When the 10 meter interconnect cable between two Model 675s is used, point-to-point diagnostics are available to verify station-to-station communications, cable data sensitivity, CRC, packet length errors, and external carrier sense. In addition to these functions, a loop-back diagnostic is provided for use with transceivers. This function is similar to the SerDes loop-back diagnostic except the transceiver cable is also verified.

Figure 2 is a block diagram of the Ethernet Communications Controller.

Software

Three levels of program interface are provided to users of the Model 675 for Ethernet software prototyping and evaluation.

MULTIBUS MESSAGE EXCHANGE (MMX)-ISIS-II

MULTIBUS Message Exchange (MMX)-ISIS-II is a simple processor-to-processor protocol which permits ISIS-II user programs to communicate with the software residing on the Ethernet Communications Controller.

The model of use of MMX is as follows: The calling program will allocate a segment of memory in the 64 Kbyte segment accessible by ISIS-II, fill in application defined fields, and transmit via MMX to a socket on the Ethernet Communications Controller. The program then waits for the application level response to the command just given. There is an MMX module in ROM on the Ethernet Communications Controller, and another in the HOST RAM.

EXTERNAL DATA LINK (EDL)

The External Data Link (EDL) presents a subset of the Data Link Layer interface to users at the MMX-ISIS-II interface level. This allows a user to write Ethernet application programs to access the Ethernet Data Link on the 8085A-2 in ISIS-II systems. The External Data Link resides in the ROM on the Ethernet Communications Controller.

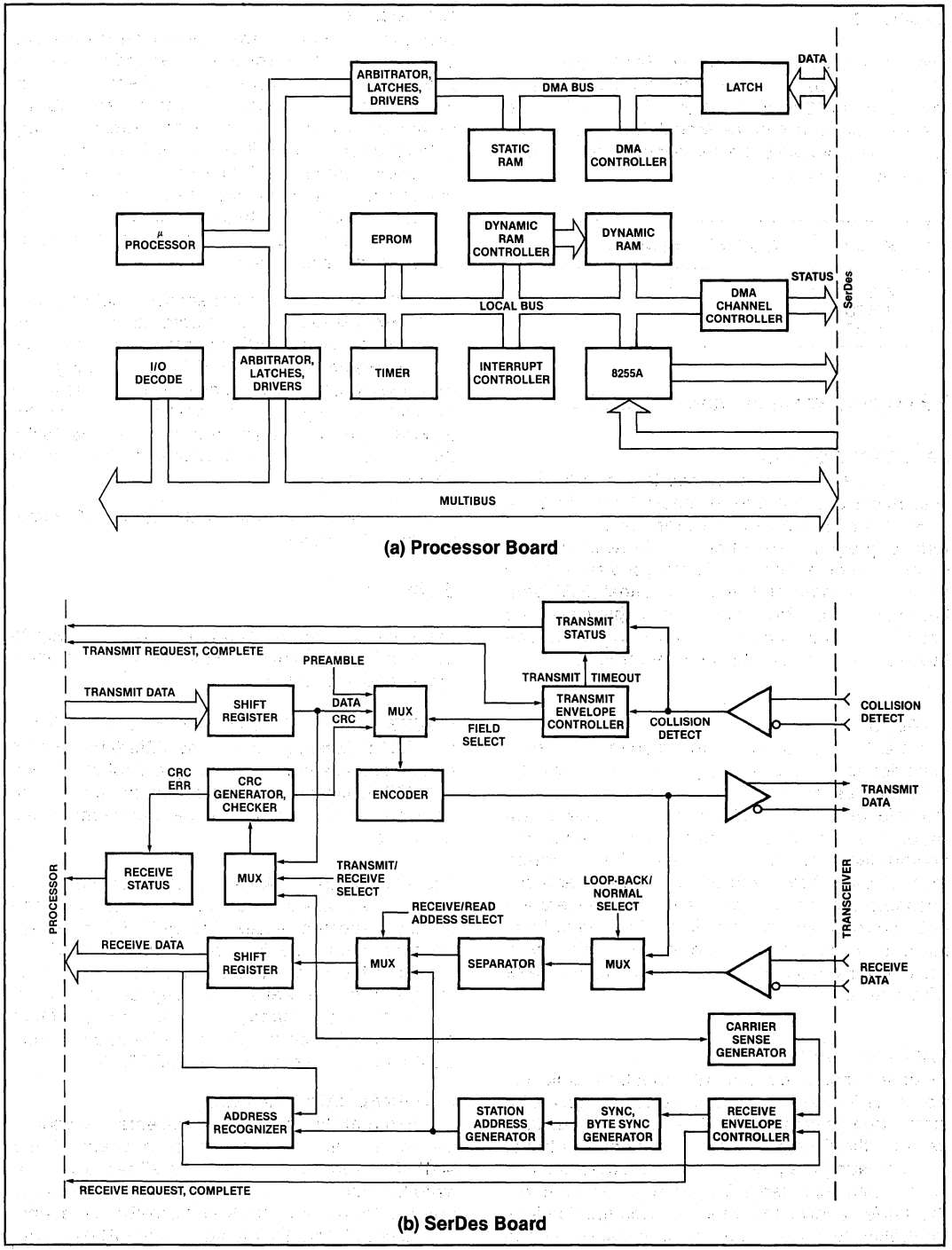


Figure 2. Block Diagram of the Ethernet Communications Controller

ETHERNET DATA LINK LIBRARY

The Ethernet Data Link Library is provided to simplify the External Data Link (EDL), MMX-ISIS-II interface. This library provides synchronous interface procedures for the EDL functions. These procedures allow the user to simply call a subroutine without being aware of the MMX-ISIS-II transaction which is made with the Ethernet Communications Controller. The Ethernet Data Link Library is provided on a diskette. It is designed to be linked with the user's software residing in the HOST RAM.

About the Ethernet

The Ethernet local area network provides a communication facility for high speed data exchange among digital devices located within a moderate sized geographic area. The Ethernet architecture defines the system as a series of independent layers.

The lowest layer, the Physical Link Layer, is concerned with the coaxial cable interface. It completely specifies the essential physical characteristics of the Ethernet, such as data encoding, timing, and voltage levels.

The Data Link defines a medium-independent link level communication facility, built on the medium-dependent physical channel provided by the Physical Layer. It supports the peer protocol statistical contention resolution (CSMA/CD), variable size frames, and link management functions.

The higher levels of the overall network architecture, which use the Data Link Layer, are collectively referred to as the Client Layer. The identity and function of this layer are user specific. The intent, however, is that the Ethernet Physical and Data Link Layers support the higher layers of the ISO model (Network Layer, Transport Layer, Session Layer, etc.).

The overall structure of the layered architecture is shown in Figure 3.

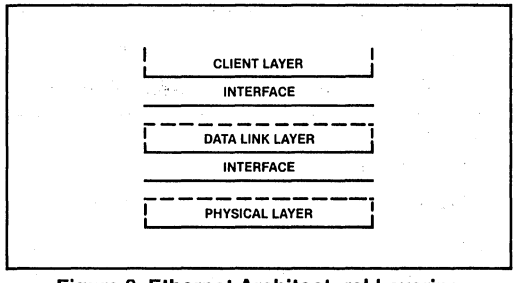


Figure 3. Ethernet Architectural Layering

DISK SUBSYSTEMS (OPTIONAL)

Dual Drive Floppy Disk Subsystem

The Model 675FD Double Density Diskette System provides direct access bulk storage, intelligent controller and two diskette drives. Each drive provides 1/2 Mbytes of storage with a data transfer of 500,000 bits/second. The controller provides an interface to the Model 675 system bus, as well as supporting up to four diskette drives to allow more than 2 Mbytes of on-line storage.

Hard Disk Subsystem

The Model 675HD Hard Disk System provides direct access bulk storage, intelligent controller and a disk drive containing one fixed platter and one removable cartridge. Each provides approximately 3.65 Mbytes of storage with a data transfer rate of 2.5 Mbits/second. The controller provides an interface to the system bus, as well as supporting up to 2 disk drives. The disk system records all data in Double Frequency (FM) on 2 surfaces per platter. Each platter can be write protected by a front panel switch.

SPECIFICATIONS

Host Processor Boards

INTEGRATED PROCESSOR CARD

—(IPC-85) 8085A-2 based, operating at 4 MHz
—64K RAM, 4K ROM (2K in monitor and 2K in boot/diagnostic)

RESIDENT PROCESSOR BOARD

—(RPB-86) 8086 based, operating at 5 MHz
—64K RAM, 16K ROM (application debugger)

BUS

—MULTIBUS system bus, maximum transfer rate of 5 MHz

DIRECT MEMORY ACCESS

—(DMA) standard capability on the MULTIBUS system bus; implemented for user selected DMA devices through optional DMA module
—Maximum transfer rate of 2 MHz

Ethernet Communications Controller

PROCESSOR
—8088 based, operating at 5 MHz
—16K dynamic RAM for program execution
—8K EPROM for program execution
—8K Static RAM for data buffer
—3 DMA channels for receive data
—1 DMA channel for transmit data

SerDes
—Serialization/Deserialization
—Framing
—CRC generation and checking
—Manchester encoding/decoding
—Destination address recognition

Integral Floppy Disk

Capacity—250 Kbytes (formatted)
Transfer Rate—160 Kbits/sec
Access Time—
- Track to Track: 10 ms max
- Average Random Positioning: 260 ns
- Rotational Speed: 360 rpm
- Average Rotational Latency: 83 ms
- Recording Mode: FM

Dual Floppy Disk Option

Capacity—
- Per Disk: 4.1 Mbits (formatted)
- Per Track: 53.2 Kbits (formatted)

Transfer Rate— 500 Kbits/sec
Access Time—
- Track to Track: 10 ms
- Head Setting Time: 10 ms
- Average Random Positioning: 260 ms
- Rotational Speed: 360 rpm
- Recording Mode: M^2 FM

Hard Disk Drive Option

Type—5440 top loading cartridge and one fixed platter
Tracks per Inch—200
Mechanical Sectors per Track—12
Recording Technique—double frequency (FM)
Tracks per Surface—400 bits/inch
Density—2,200 bits/inch
Bits per Track—62,500
Recording Surfaces per Platter—2
Capacity—
- Per Surface—15 Mbits
- Per Platter—29 Mbits
- Per Drive—59 Mbits
- Per Drive—7.3 Mbytes (formatted)

Transfer Rate—2.5 Mbits/sec
Access Time—
- Track to Track: 13 ms max
- Full Stroke: 100 ms
- Rotational Speed: 2,400 rpm

Physical Characteristics

Width—17.37 in. (44.12 cm)
Height—15.81 in. (40.16 cm)
Depth—19.13 in. (48.59 cm)
Weight—84.5 lb. (38.6 kg)

Expansion Chassis

Width—17.37 in. (44.12 cm)
Height—4.81 in. (17.22 cm)
Depth—19.13 in. (48.59 cm)
Weight—42 lb. (19 kg)

Keyboard

Width—17.37 in. (44.12 cm)
Height: 3.0 in. (22.86 cm)
Depth—9.0 in. (22.86 cm)
Weight—6 lb. (3 kg)

Dual Floppy Drive System (Option)

Width—16.88 in. (42.88 cm)
Height—12.08 in. (30.68 cm)
Depth—1.0 in. (48.26 cm)
Weight—64 lb. (29 kg)

Hard Disk Drive System (Option)

Width—18.5 in. (47.0 cm)
Height—34.0 in. (86.4 cm)
Depth—29.75 in. (75.6 cm)
Weight—202 lb. (92 kg)

ELECTRICAL CHARACTERISTICS

DC Power Supply for Mainframe

Volts Supplied	Amps Supplied	Typical System Requirements
+5 ± 5%	30.0	17.0
+12 ± 5%	2.5	1.1
−12 ± 5%	0.3	0.1
−10 ± 5%	1.0	0.08
+15 ± 5%*	1.5	1.5
+24 ± 5%*	1.7	1.7

*Not available on bus.

AC Requirements for Mainframe

110V, 60 Hz—5.9 Amp
220V, 50 Hz—3.0 Amp

DC Power Supply for Expansion Chassis

Volts Supplied	Amps Supplied	Typical System Requirements
+5 ± 5%	24	None
+12 ± 5%	2.0	None
−12 ± 5%	0.3	None
−10 ± 5%	1.0	None

AC Requirements for Expansion Chassis

50-60 Hz, 115/230V AC

ENVIRONMENTAL CHARACTERISTICS

System Operating Temperature—16°C to 32°C (61°F to 90°F)
Humidity—20% to 80%

DOCUMENTATION SUPPLIED

Ethernet Communications Controller Programmer's Reference Manual, 121769.

Ethernet Development System Upgrade Kit Installation and Checkout Manual, 121778.

Intellec Series III Microcomputer Development System Product Overview, 121575.

Intellec Series III Microcomputer Development System Console Operating Instructions, 121609.

Intellec Series III Microcomputer Development System Pocket Reference, 121610.

Intellec Series III Microcomputer Development System Programmer's Reference, 121618.

iAPX 88/86 Family Utilities User's Guide for 8086-Based Development Systems, 121616.

8086/8087/8088 Macro Assembly Language Reference Manual for 8086-Based Development Systems, 121627.

8086/8087/8088 Macro Assembly Language Pocket Reference, 9800/49.

8086/8087/8088 Macro Assembler Operating Instructions for 8086-Based Development Systems, 121628.

Intellec Series III Microcomputer Development System Installation and Checkout Manual, 121612.

Intellec Series III Microcomputer Development System Schematic Drawings, 121642.

ISIS-II CREDIT (CRT-Based Test Editor) User's Guide, 9800902.

ISIS-II CREDIT (CRT-Based Test Editor) Pocket Reference, 9800903.

The 8086 Family User's Manual, 9800722.

The 8086 Family User's Manual, Numeric Supplement, 121586.

For Series III Plus Hard Disk System Only:

Model 740 Hard Disk Subsystem Operation and Checkout, 9800943.

ORDERING INFORMATION

Part Number	Description
DS675A KIT	Intellec Model 675 Development System for Ethernet (110V/60 Hz)
DS675B KIT	Intellec Model 675 Development System for Ethernet (220V/50 Hz)
DS675AFD KIT	Intellec Model 675 Development System for Ethernet with Dual Density Flexible Disk System (110V/60 Hz)
DS675BFD KIT	Intellec Model 675 Development System for Ethernet with Dual Density Flexible Disk System (220V/60 Hz)
DS675AHD KIT	Intellec Model 675 Development System for Ethernet with Pedestal Mounted Hard Disk (110V/60 Hz)
DS675BHD KIT	Intellec Model 675 Development System for Ethernet with Pedestal Mounted Hard Disk (220V/50 Hz)

All models listed above require a Software License.